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Design and Analysis of Power consumption comparison of Adiabatic and Conventional CMOS logic circuits

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Abstract: Power consumption plays an important role in the performance analysis of an electronic circuits and devices. Present day electronic devices are portable and they require more battery backup, this can be achieved by designing the circuits such that the power dissipation should be less. It can be reduced by using different design technology, one of the most commonly used VLSI technology is CMOS technology. In this project, One efficient technology called Adiabatic technology is used for overcome the limitations of CMOS technology for reducing the power dissipation without degrading the performance of the device. In the proposed paper, Different circuits using Adiabatic technology and CMOS technology will be designed and simulated on Hspui G-2012.06-SP1 using HSPICE language and shall be verified with the help of its simulation result.

Keywords: CMOS, Conventional switching, Adiabatic logic, Adiabatic switching

1.INTRODUCTION

Adiabatic logic is also called efficient charge recovery logic or reversible logic. The term 'Adiabatic' is refers to the thermodynamic process that exchanges no heat with the environment. CMOS Logic styles have been extremely successful in both technically as well as in terms of market share but switching power, dissipation of CMOS circuit with capacitive load has a lower limit, this limitation can be overcome by using the circuits which is designed adiabatically. it also allow the recycling of energy to reduce the total energy drawn from the power supply.

Number of transistor for a given chip area is increased with the technological evolution there by increases the switching cycle from MHz to GHz. Programmable reversible logic is a prospective design style for implementation of low power low frequency application where minimum heat dissipation is possible. It can be possible by using adiabatic technology [1][2][3].

In this proposed paper design a power efficient, high precision, high performance and accurate logic circuits using adiabatic logic and which is compared with same logic circuits designed by using CMOS technology on Hspui G-2012.06-SP1 using HSPICE language. Simulation result can be verified using custom explorer as well as CosmosScope.

2. CONVENTIONAL CMOS AND ADIABATIC TECHNOLOGY

2.1 Conventional CMOS technology

One of the most popular MOSFET technologies available today is the complementary MOS, or CMOS, technology. This technology makes use of both P and N channel devices in the same substrate material. Such devices are extremely useful, since the same signal, which turns on a transistor of one type, is used to turn off a transistor of the other type. This allows the design of logic devices using only simple switches, without the need for a pull-up resistor.Power loss in conventional CMOS transistors mainly occurs because of device switching. Figure2.1.a shows a typical inverter implementation which shows actual charging and discharging processes in CMOS technology.

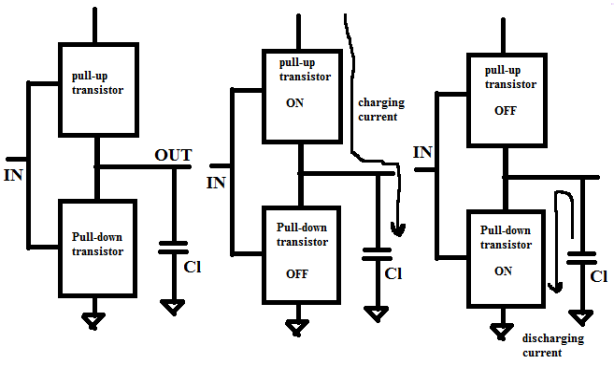

Figure2.1.a Charging and discharging in CMOS

1. It uses symmetric pull up and pull down transistors.
2. Load capacitor start to charge when pull-up transistor is ON.
3. Energy stored in the load capacitance is discharge to ground when pull-down transistor is ON. Whatever energy is stored by the capacitor at the time of charging is dissipated to the ground.

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The operation of the circuit can be evaluated in two stages of charging phase and discharging phase. During the charging phase shown in figure2.1.a, the input to the circuit is logic LOW. During this phase, the PMOS transistor conducts and NMOS transistor goes in to OFF state which charges the output value to power supply results in logic HIGH output.

During the discharging phase shown in figure2.1.a,the input to the circuit is logic HIGH. During this phase, the NMOS transistor conducts and PMOS transistor goes into OFF state, which results in a discharging path from output terminal to ground. So when input is high will get Low output and when the input is Low will get High output.the simulation waveform is shown in figure 2.1.b

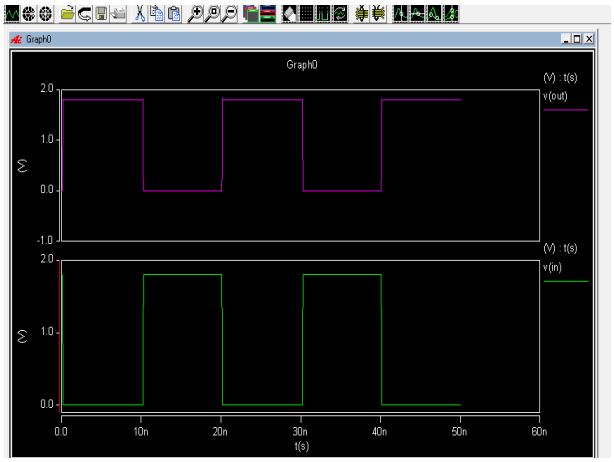

figure 2.1.b Simulation waveform

2.2.Adiabatic technology

The word ADIABATIC is derived from the Greek word "adiabatos",which means there is no exchange of energy with the environment and hence no energy loss in the form of heat dissipation. Adiabatic logic is commonly used to reduce the energy loss during the charging and discharging process of circuit operation. Adiabatic logic is also known as "energy recovery" or "charge recovery" logic.

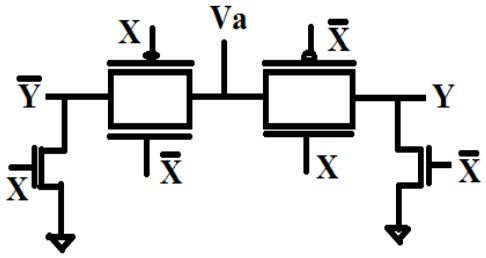

Figure2.2.a Adiabatic Circuit

Adiabatic circuit design is shown in figure 2.2.a

1. It consists of two transmission gates and two NMOS clamps.
2. Input and outputs are dual rail encoded to avoid the use of inverters.
3. Depending on the valid input value, amplifier is energized by a slow voltage ramp from zero to Vdd. Next the amplifier is de-energized by ramping the voltage on Vdd back to zero keeping the input pair constant.

2.3Adiabatic Switching

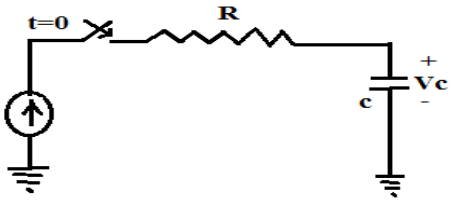

Figure2.3.a adiabatic switching

Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small [5]. This can be achieved by charging the capacitor from a time varying voltage source or constant current source, as shown in Figure 2.3. Here, R represents the on-resistance of the pMOS network. Also note that a constant charging current corresponds to a linear voltage ramp. Assuming that the capacitance voltage VC is zero initially, the variation of the voltage as a function of time can be found as

$$VC(t)=IS.tC \quad (1)$$

Hence the charging current can be expressed as a function of VC and time t

$$IS=C.VC(t)t \quad (2)$$

The amount of energy dissipated in the resistor R from t = 0 to *t* = T can be found as

$$Ediss=R\int Is2dt=RIs2T \quad (3)$$

Combining (2) and (3), the dissipated energy during this charge-up transition can also be expressed as

$$Ediss=RC/T.CVc2(T) \quad (4)$$

From (4) we can say that the dissipated energy is smaller than for the conventional case if the charging time T >>2RC and can be made small by increasing the charging time. A portion of the energy thus stored in the capacitance can also be reclaimed by reversing the current source direction, allowing the charge to be transferred from the capacitance back into the supply. Adiabatic logic circuits thus require non-standard power supplies with time-varying voltage, also called pulsed power supplies.

3.CONVENTIONAL CMOS AND ADIABATIC LOGIC CIRCUITS

3.1 AND Gate

An AND gate output rise only when it's all inputs are high(1).AND gate circuit diagram in CMOS and adiabatic logic is shown in figure 3.1 (a) and (b) and its simulation wave form shown in figure 3(c)

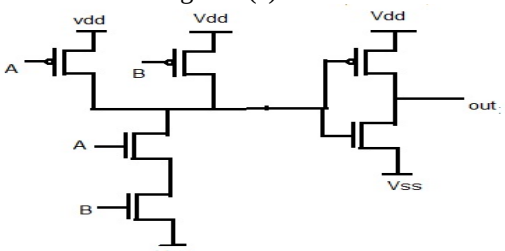

Figure3.1.a. Conventional CMOS AND gate

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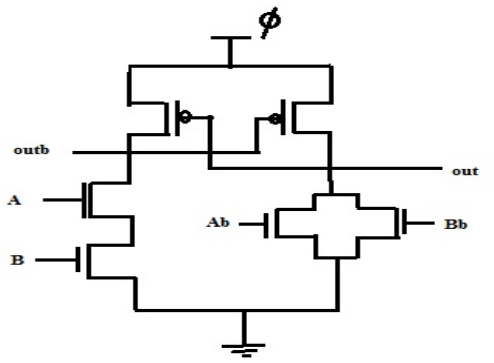

Figure3.1.b. Conventional CMOS AND gate

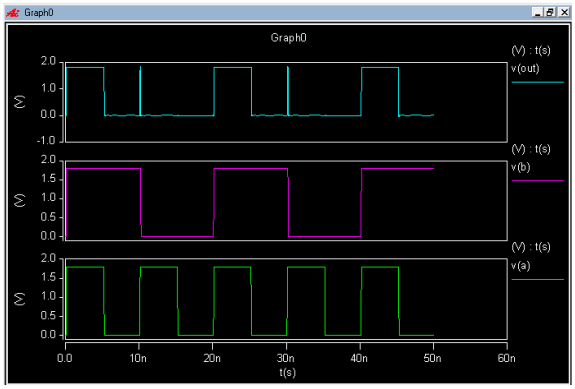

Figure 3.1.c.simulation waveform of AND gate

3.2 OR Gate

An OR gate output is fall only when it's all inputs are low(0)**.** AND gate circuit diagram in CMOS and adiabatic logic is shown in figure3.2(a) an (b) and its simulation wave form shown in figure3.2(c)

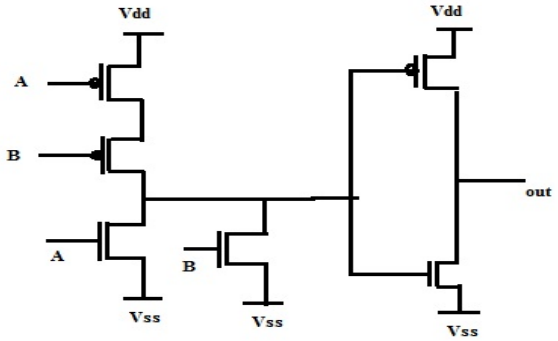

Figure3.2.a. Conventional CMOS OR gate

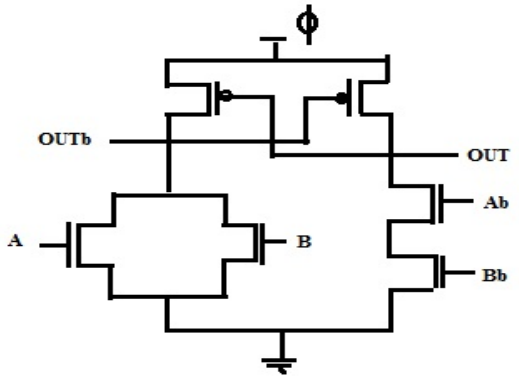

Figure3.2.b. Adiabatic OR gate

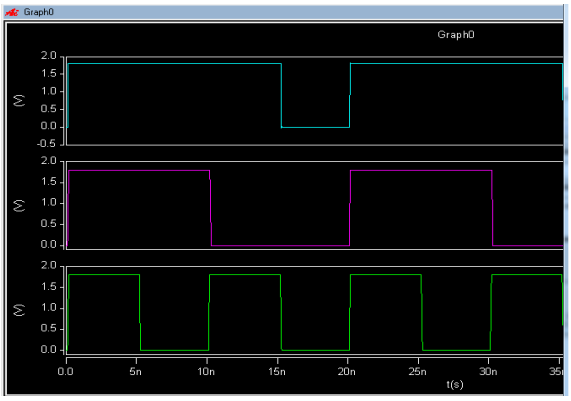

Figure 3.2.c.simulation waveform of OR gate

3.3 Half Adder

Adders are combinations of logic gates that combine binary values to obtain a sum. They are classified according to their ability to accept and combine the digits.
Half Adder: is a combinational circuit that performs the addition of two bits, this circuit needs two binary inputs and two binary outputs. truth table is shown in table 3.3.a, Figure3.3a and 3.3.b shows construction of a half adder using conventional and adiabatic logic respectively.

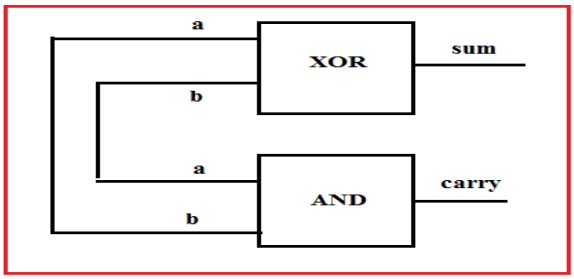

Figure3.3a Half adder using Conventional CMOS gates

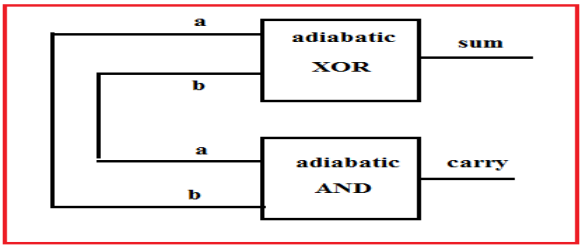

Figure3.3a Half adder using adiabatic gates

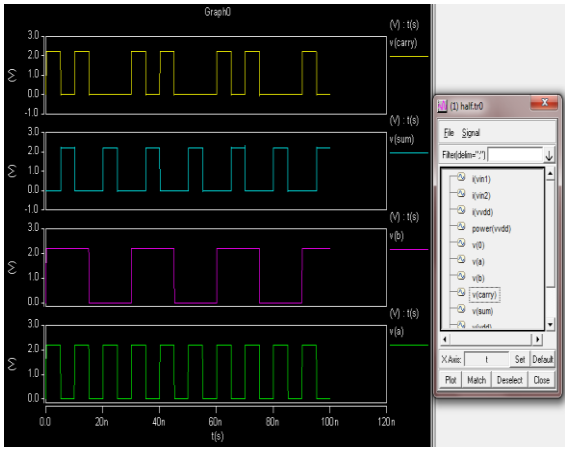

Figure3.3a Half adder Simulation waveform

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Table 3.3 truth table of half adder

INPUT		OUTPUT	
a	b	sum	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

3.4 Full Adder

The full adder becomes necessary when a carry input must be added to the two binary digits to obtain the correct sum. A half adder has no input for carries from previous circuits. One method of constructing a full adder is to use two half adders and an OR gate as shown in figure3.4.(a)and (b) The inputs A and B are applied to gates 1 and 2. These make up one half adder. The sum output of this half adder and the carry-from a previous circuit become the inputs to the second half adder. The carry from each half adder is applied to gate 5 to produce the carry-out for the circuit.

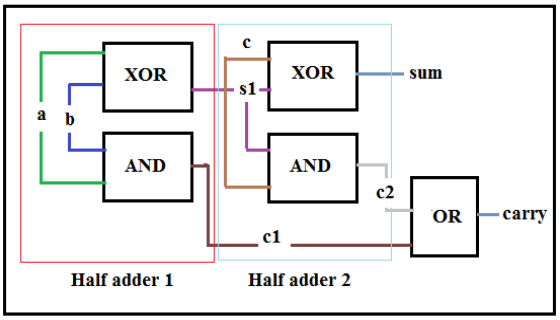

Figure3.4.a Full adder using conventional CMOS

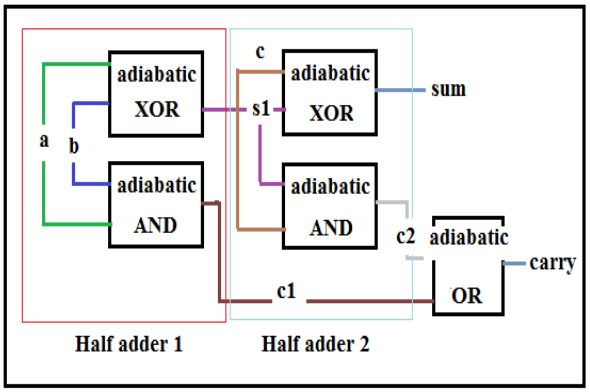

Figure3.4.b.Full adder using Adiabatic logic

Table3.4.truth table of Full adder

INPUT			OUTPUT	
a	b	c	sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

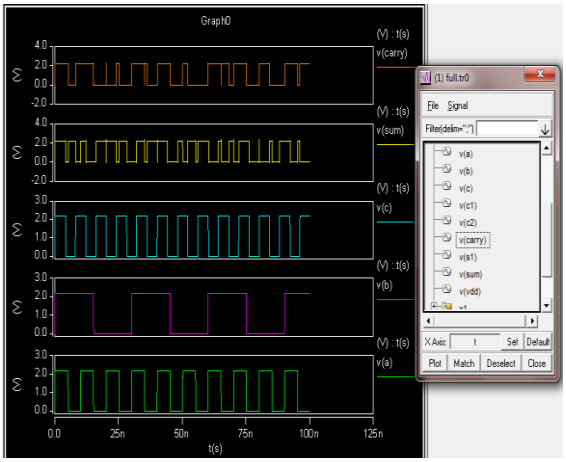

Figure3.4.c full adder Simulation waveform

4.DESIGN AND ANALYSIS OF MULTIPLIER

The combinational structure of the standard multiplier is shown in figure4.a, instead of registers it comprises of CMOS/ Adiabatic logic gates. The unit takes two 2 bit inputs A(A0,A1) and B(B0,B1) and produce a 4 bit output (Cout,S2,S1,S0)

A1 A0
B1 B0

N1 N0
N3 N2

Cout S2 S1 S0

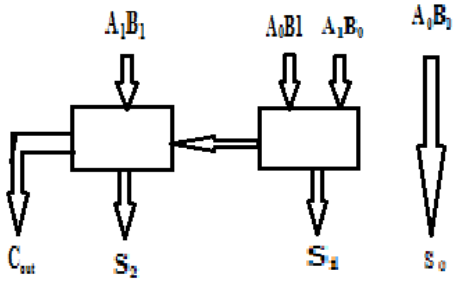

Figure 4.a.Architecture of multiplier

Simulation result of 2X2 multiplier [1] using conventional CMOS gates and Adiabatic logic are shown in figure4. (b) and (c).

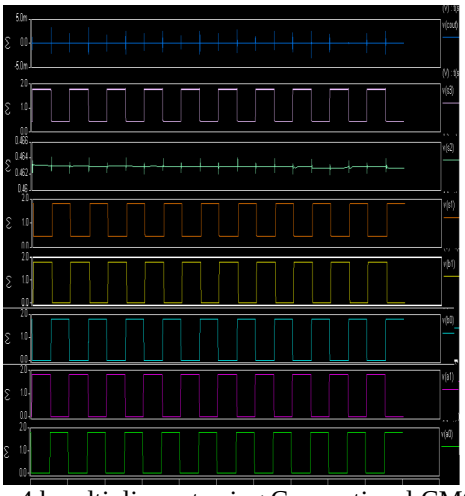

Figure4.bmultiplier out using Conventional CMOS

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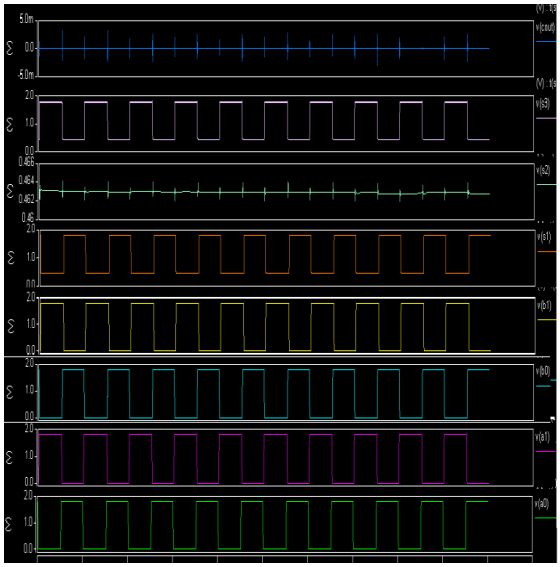

Figure4.c.multiplier out using Adiabatic logic

5.HSPICE

A. Hspui G-2012.06-SP1 is used for simulation of this proposed design style by using HSPICE language.

B. Some important features of HSPICE are:

1. Superior Convergence.
2. Accurate modeling including many foundry models.
3. Circuit optimization for models and cells, with incremental or simultaneous multiparameter optimization in AC,DC ,and transient analysis.

SPICE (Simulation Program with Integrated Circuit Emphasis) is a general-purpose, analog electronic circuit simulator. It is a powerful program that is used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behavior. It is also used to simulate digital circuit. SPICE is a widely used tool for simulating electrical circuits.

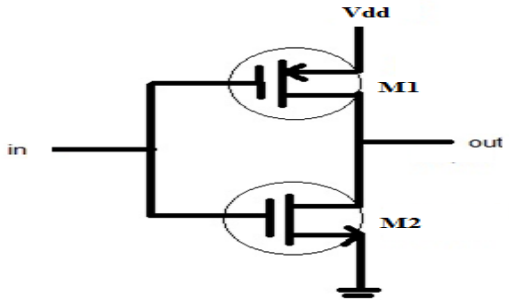

Figure 5.a.inverter

The HSPICE netlist describing an inverter circuit is:

```
.OPTION POST
 .include tsmc018um.txt
.model nch nmos
.model pch pmos
m1 out in vdd vdd  pch l=180nm w=2u
m2 out in gnd gnd  nch l=180nm w=1u
vin in gnd pulse 1.8v 0v 0.1n 0.1n 0.1n 10ns 20ns
v1 vdd gnd dc 1.8v
.tran 1ns 50ns
.measure tran AVG_Power avg p(v1) from 1ns to 50ns
.measure power AVG POWER FROM=1ns TO=50ns
.measure tran average_delay param='(tphl+tplh)/2'
.end
```

The PMOS and NMOS transistors are given the names m1 and m2 respectively. Two lines

```
m1 out in vdd vdd  pch l=180nm w=2u
m2 out in gnd gnd  nch l=180nm w=1u
```

describe the connection of the drain, gate, source, and bulk(substrate) terminals, the name of the HSPICE model used to describe electrical characteristics of the transistor, and the length and width of the channel. That is the transistor labeled m1 in the circuit (and the netlist) has its drain terminal connected to the node labeled OUT, the gate terminal connected to node IN, both the source and substrate terminals are connected to the node labeled Vdd.The name of the HSPICE mosfet model used to describe this transistor's electrical parameters is PCH. The two .MODEL lines tell HSPICE which transistor model to use. In this case, we are using two basic models called PCH and NCH.

➢ Open the file netlist file (.sp) ,then simulate.

This will run the HSPICE simulator, reading in the commands in the file inverter.sp and generating an output file called inverter.lis. In addition, several intermediate files will be created which will be used by the AwanWaves or cosmosScope tool to display the simulation results.

Once the simulation completes, the following message will be printed:

>info: ***** hspice job concluded

➢ Examine the inverter.lis file.

It will contain a listing of the voltages at nodes IN and OUT, All parameters specifications result of transiant analysis ect. If threre is any error ti is displed in the list file, which can be edited by using edit netlist file.

➢ To view the simulation results using the Synopsys open file .tr0 in cosmosscope as shown in figure5.c

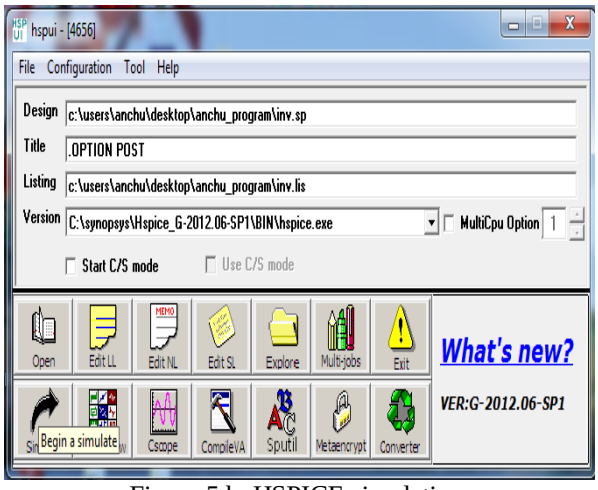

Figure 5.b. HSPICE simulation

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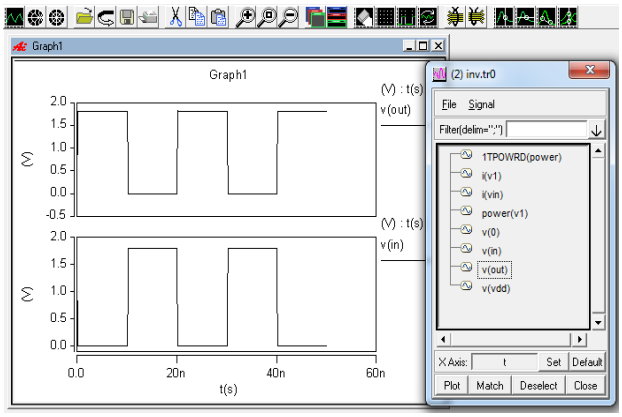

Figure 5.c.Simulation result in CosmosScope

5.1 Comparison Of power consumption for conventional and adiabatic CMOS Gates/Circuits CMOS

Table 5.1 power consumption analysis

Gate/Circuit	Power Consumption	
	CMOS logic	Adiabatic logic
Inverter	183.4915nw	10.0277nw
AND	373.62nw	5.1034nw
NAND	240.8043nw	
OR	177.118nw	7.977nw
NOR	124.3307n	
Half Adder	2.0806u	979.1601n
Full Adder	5.4368u	1.0000u
2X2 Multiplier	8.4450uw	1.8027uw

6.CONCLUSION

In the proposed paper different circuits, using both adiabatic logic and conventional CMOS logic is designed. The design is modeled using HSPICE and simulated with the help of Hspui G-2012.06-SP1.An efficient, accurate, precise device can be generated with very less power dissipation without degrading the performance of the device. The analysis shows that designs based on adiabatic principle gives superior performance when compared to traditional approaches in terms of power even though their transistor count is high in some circuits so for low power and ultra low power requirements adiabatic logic is an effective alternative for traditional CMOS logic circuit design. This comparison is done by using HSPICE simulator Hence, it is concluded that the proposed design circuit will provide a platform for designing high performance and low power digital circuits such as digital signal processors, adders and multiplexers ,multiplier etc. HSPICE can be used for both analog and digital circuit for getting more precise and accurate result. This technology can be used in electronic communication technology where both encryption and decryption is needed because of the reversible feature of adiabatic logic.

REFERENCES

[1]. Matthew Morrison,and Nagarajan Ranganathan "Synthesis of Dual-Rail Adiabatic Logic for Low Power Security Applications" IEEE transactions on computer-aided design of integrated circuits and systems, vol. 33, no. 7, July 2014.

[2]. Thockchom Birjit Sinha, Shruti Konwar,Soumik Roy,"Low Power Design and analysis of Fundamental Logics using Adiabatic Array Logic". IEEE transactions 2014.

[3]. Anu Priya,Amrita rai,"Adiabatic Technique for power efficient logic circuit design",IJECT Vol.5,Issue Spl-1,Jan-March 2014.

[4]. Amit Saxena,Deepti Shinghal,Arti Noor "Power efficient Adiabatic Switching Circuits",MIT International journal of electronics and Communication Engineering, Vol. 3.No.2,August 2013.

[5] Samik Samanta, Rajat Mahapatra, Ashis Kumar Mal "EFFICIENT ENERGY RECOVERY LOGIC: STUDY AND IMPLEMENTATION", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering,Vol. 2, Issue 9, September 2013

[6]. P. Teichmann, Fundamentals of Adiabatic Logic Adiabatic Logic, Springer Series in Advanced Microelectronics 34,Springer Science+Business Media B.V. 2012.

[7]. Y.Xu and A.Srivastava,"New Energy Recovery CMOS XNOR&XOR Gates", IEEE transactions 2007.

[8]. Version, HSPICE® Simulation and Analysis User Guide, March 2006.

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